**RAMA KRISHNA YARRAMSETTI**

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**Career Objective:**

An enthusiastic and self-motivated looking for a challenging and responsible position as **Physical design engineer** to apply my knowledge and skill with my hard work and patience.

**Academic Chronicle:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Course** | **Institution** | **Board/University** | **Year** | **Percentage** |
| **B.Tech (ECE)** | Swarnandhra College Of  Engineering &Technology(Autonomous), Narsapur. | JNTUK | 2022 | **8.12**  CGPA |
| Inter | Vignan junior College,Mandapeta | Board of intermediate,AP | 2018 | **88.6%** |
| SSC | ST.Anna’s school | State Board of Secondary Education,AP | 2016 | **9.2**  CGPA |

**Core Competency :**

* Hands on technical expertise in Block level physical design implementation.
* Good knowledge of VLSI design flow -**ASIC design flow** (**RTL to GDS II)**
* Hands on experience in **synthesis, sanity checks.**
* Hands on experience in **PNR** flow using ICC2, Design Compiler tools by Synopsys**.**
* Having technical exposure on Floor Planning, Place and route, Clock Tree Synthesis, Timing Analysis, DRC/LVS, Crosstalk analysis, IR drop analysis
* Good knowledge of **MOSFET, CMOS** and its operations in different regions**.**
* Having technical exposure On **CMOS VLSI Digital Design.**
* Good knowledge on Digital Electronics.

**TECHNICAL SKILLS:**

* Tools used

P&R : Synopsys ICCII

Synthesis : Design compiler

STA : Prime time

RC extraction : Starrc

* Scripting language : Tcl , python
* Operating system : windows,linux/unix
* Programming language : c ,c++ , java , python
* Digitals electronics ,Verilog , Embedded systems , IOT , MS office .

**PROFESSIONAL TRAINING**

**Physical Design** Training from **VLSIGURU** Training Institute Bengaluru, Karnataka 560043,

for 6 months.

**Project Experience: project 1**

Technology/Layers : 28nm / 9 Metal layers

Design Name. : 32 bit processor (ORCA TOP)

Macros : 40

STD cells : 52007

No. of clocks : 2+3+3

Target clock Frequency : 450MHz

**⮚ Objectives**

● Imported verilog netlist, read SDC, and linked libraries.

● Performed sanity checks and did various iterations of floorplanning.

● Creating the floorplan with high importance for optimum performance.

● During TR1, did various floorplanning with given Def and also by changing size of the block to get desired timing and congestion with reducing area.

● Pin placement was done with the help of guidelines given by top level.

● Place & route the design for meeting requirement.

● Applied various strategies to reduce skew and latency in cts stage.

● Fixed trans and timing violations and analyzed antenna violations and cross talk.

● Fixing post route issues using ECO.

● Performed sign-off and closed the timing using primetime

**Project Experience: project 2**

Technology/Layers : 28nm / 9 Metal layers

Macros : 24

STD cells : 350K

No. of clocks : 4

Target clock Frequency : 720MHz

Role : The tasks handled were Block level floor planning, End cap

Insertion, Tap cell insertion, Placement, Post placement timing

Closure, Clock tree synthesis, Post clock Timing closure, clock skew

Fixing, Timing fixing & Fixing DRCs.

**⮚ Objectives**

● Creating the floorplan with high importance for optimum performance.

● Place & route the design for meeting requirement.

● Fixing post route issues using ECO.

**Certifications :**

* Participated in the workshop “Problem Solving and Programming In Python” by APSSDC, at Swarnandhra College of engineering and technology.
* Completed internship on “**Embedded system**“ by APSSDC, at Swarnandhra College of engineering and technology.
* Completed 3 months internship on “Java/j2EE concept” at wipro.

**Academic Project :**

*Title* : “Fully automated family robort ” .

*Description* : The fully automated family robot using IoT ensure to minimize the risk of human loss and property.This project will detects the fire, gas and metal things with real time monitoring,if any abnormal value is sensed by the sensors, then buzzer will blow on this project and at the same data will send to IoT cloud.

**Strengths:**

* Teamwork
* Emotional Intelligence
* Communication Skills
* Leadership

**Declaration**

I hereby declare that the information furnished above is true to the best of my knowledge.

**Place:**

**Date:**

**(RAMA KRISHNA YARRAMSETTI)**